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ISOLATION REGION FORMING METHODS

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Isolation Region Forming Methods

TECHNICAL FIELD

The invention pertains to methods of forming isolation regions and can have particular application to methods of forming shallow trench isolation regions.

BACKGROUND OF THE INVENTION

In modern semiconductor device applications, numerous individual devices are packed onto a single small area of a semiconductor substrate. Many of these individual devices need to be electrically isolated from one another. One method of accomplishing such isolation is to form a trenched isolation region between adjacent devices. Such trenched isolation region will generally comprise a trench or cavity formed within the substrate and filled with an insulative material, such as, for example, silicon dioxide. Trench isolation regions are commonly divided into three categories: shallow trenches (trenches less than about one micron deep); moderate depth trenches (trenches of about one to about three microns deep); and deep trenches (trenches greater than about three microns deep).

Prior art methods for forming trench structures are described with reference to Figs. 1-12. Referring to Fig. 1, a semiconductor wafer fragment 10 is shown at a preliminary stage of a prior art processing

sequence. Wafer fragment 10 comprises a semiconductive material 12 upon which is formed a layer of oxide 14, a layer of nitride 16, and a patterned layer of photoresist 18. Semiconductive material 12 commonly comprises monocrystalline silicon which is lightly doped with a conductivity-enhancing dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Oxide layer 14 typically comprises silicon dioxide, and nitride layer 16 typically comprises silicon nitride. Nitride layer 16 is generally from about 400 Angstroms thick to about 920 Angstroms thick.

Referring to Fig. 2, patterned photoresist layer 18 is used as a mask for an etching process. The etch is typically conducted utilizing dry plasma conditions and $\text{CH}_2\text{F}_2/\text{CF}_4$ chemistry. Such etching effectively etches both silicon nitride layer 16 and pad oxide layer 14 to form openings 20 extending therethrough. Openings 20 comprise peripheries defined by nitride sidewalls 17 and oxide sidewalls 15. The etching stops upon reaching silicon substrate 12.

1 Referring to Fig. 3, a second etch is conducted to extend
2 openings 20 into silicon substrate 12. The second etch is commonly
3 referred to as a "trench initiation etch." The trench initiation etch is
4 typically a timed dry plasma etch utilizing CF_4/HBr , and typically extends
5 openings 20 to less than or equal to about 500 Angstroms into
6 substrate 12. A purpose of the trench initiation etch can be to clean
7 an exposed surface of silicon substrate 12 within openings 20 (i.e., to
8 remove defects and polymer material) prior to final trenching into
9 substrate 12. Another purpose of the trench initiation etch can be to
10 form polymer over exposed sidewall edges 15 and 17 of oxide layer 14
11 and nitride layer 16, respectively. Such polymer can alleviate erosion of
12 sidewall edges 15 and 17 during subsequent etching of substrate 12.

13 Referring to Fig. 4, a third etch is conducted to extend
14 openings 20 further into substrate 12 and thereby form trenches within
15 substrate 12. Extended openings 20 comprise a periphery 22 defined by
16 substrate 12. The third etch typically utilizes an etchant consisting
17 entirely of HBr , and is typically a timed etch. The timing of the etch
18 is adjusted to form trenches within substrate 12 to a desired depth. For
19 instance, if openings 20 are to be shallow trenches, the third etch will
20 be timed to extend openings 20 to a depth of less than or equal to
21 about one micron.

22 Referring to Fig. 5, photoresist layer 18 (Fig. 4) is removed and
23 a first oxide layer 24 is thermally grown within openings 20 and along

1 the periphery 22 (Fig. 4) defined by silicon substrate 12. The growth
2 of oxide layer 24 can form small bird's beak regions 26 underlying
3 sidewall edges 17 of nitride layer 16.

4 Referring to Fig. 6, a high density plasma oxide 28 is formed to
5 fill openings 20 (Fig. 5) and overlie nitride layer 16. High density
6 plasma oxide 28 merges with oxide layer 24 (Fig. 5) to form oxide
7 plugs 30 within openings 20 (Fig. 5). Oxide plugs 30 have laterally
8 outermost peripheries 33 within openings 20.

9 Referring to Fig. 7, wafer fragment 10 is subjected to planarization
10 (such as, for example, chemical-mechanical polishing) to planarize an
11 upper surface of oxide plugs 30. The planarization stops at an upper
12 surface of nitride layer 16.

13 Referring to Fig. 8, nitride layer 16 is removed to expose pad
14 oxide layer 14 between oxide plugs 30.

15 Referring to Fig. 9, pad oxide layer (Fig. 8) is removed. The
16 removal of the pad oxide layer leaves dips 32 at edges of oxide
17 plugs 30.

18 Referring to Fig. 10, a sacrificial oxide layer 34 is grown over
19 substrate 12 and between oxide plugs 30.

20 Referring to Fig. 11, sacrificial oxide layer 34 (Fig. 10) is removed.
21 Formation and removal of sacrificial oxide layer 34 can be utilized to
22 clean a surface of substrate 12 between oxide plugs 30. As such surface
23 of substrate 12 can be ultimately utilized to form an active area of a

1 transistor device, it is desired that the surface be substantially free of
2 defects. The removal of sacrificial oxide layer 34 can also undesirably
3 exacerbate dips 32.

4 Referring to Fig. 12, a silicon dioxide layer 36 is regrown between
5 oxide plugs 30, and a polysilicon layer 38 is formed over oxide plugs 30
6 and oxide layer 36. Polysilicon layer 38 can ultimately be formed into
7 a word line comprising transistor gate regions. Such transistor gate
8 regions can lie between oxide plugs 30. Plugs 30 can then function as
9 trenched isolation regions between transistor devices. Dips 32 can
10 undesirably result in formation of parasitic devices adjacent the transistor
11 devices and ultimately have an effect of lowering a threshold voltage for
12 the transistor devices. Accordingly, it would be desirable to alleviate
13 dips 32. Dips 32 can also interfere with subsequent fabrication processes
14 and, for this reason as well, it would be desirable to alleviate dips 32.

15 16 SUMMARY OF THE INVENTION

17 In one aspect, the invention encompasses an isolation region
18 forming method. An oxide layer is formed over a substrate. A nitride
19 layer is formed over the oxide layer. The nitride layer and oxide layer
20 have a pattern of openings extending therethrough to expose portions of
21 the underlying substrate. The exposed portions of the underlying
22 substrate are etched to form openings extending into the substrate.
23 After etching the exposed portions of the substrate, portions of the

1 nitride layer are removed while leaving some of the nitride layer
2 remaining over the substrate. After removing portions of the nitride
3 layer, oxide is formed within the openings in the substrate. The oxide
4 within the openings forms at least portions of isolation regions.

5 In another aspect, the invention encompasses another embodiment
6 isolation region forming method. A silicon nitride layer is formed over
7 a substrate. A masking layer is formed over the silicon nitride layer.
8 A pattern of openings is formed to extend through the masking layer
9 and to the silicon nitride layer. The openings are extended through the
10 silicon nitride layer to the underlying substrate. The silicon nitride layer
11 has edge regions proximate the openings and has a central region
12 between the edge regions. The openings are extended into the
13 underlying substrate. After extending the openings into the underlying
14 substrate, a thickness of the silicon nitride layer is reduced at the edge
15 regions to thin the edge regions relative to the central region. Oxide
16 is formed within the openings that are extended into the substrate. The
17 oxide within the openings forms at least portions of isolation regions.

1 **BRIEF DESCRIPTION OF THE DRAWINGS**

2 Preferred embodiments of the invention are described below with
3 reference to the following accompanying drawings.

4 Fig. 1 is a diagrammatic, fragmentary, cross-sectional view of a
5 semiconductor wafer fragment at a preliminary step of a prior art
6 processing sequence.

7 Fig. 2 shows the Fig. 1 wafer fragment at a prior art processing
8 step subsequent to that of Fig. 1.

9 Fig. 3 shows the Fig. 1 wafer fragment at a prior art processing
10 step subsequent to that of Fig. 2.

11 Fig. 4 shows the Fig. 1 wafer fragment at a prior art processing
12 step subsequent to that of Fig. 3.

13 Fig. 5 shows the Fig. 1 wafer fragment at a prior art processing
14 step subsequent to that of Fig. 4.

15 Fig. 6 shows the Fig. 1 wafer fragment at a prior art processing
16 step subsequent to that of Fig. 5.

17 Fig. 7 shows the Fig. 1 wafer fragment at a prior art processing
18 step subsequent to that of Fig. 6.

19 Fig. 8 shows the Fig. 1 wafer fragment at a prior art processing
20 step subsequent to that of Fig. 7.

21 Fig. 9 shows the Fig. 1 wafer fragment at a prior art processing
22 step subsequent to that of Fig. 8.
23

1 Fig. 10 shows the Fig. 1 wafer fragment at a prior art processing
2 step subsequent to that of Fig. 9.

3 Fig. 11 shows the Fig. 1 wafer fragment at a prior art processing
4 step subsequent to that of Fig. 10.

5 Fig. 12 shows the Fig. 1 wafer fragment at a prior art processing
6 step subsequent to that of Fig. 11.

7 Fig. 13 is a schematic, fragmentary, cross-sectional view of a
8 semiconductor wafer fragment in process according to a first embodiment
9 method of the present invention. The processing step illustrated in
10 Fig. 13 is subsequent to the prior art processing step shown in Fig. 3.

11 Fig. 14 shows the Fig. 13 wafer fragment at a processing step
12 subsequent to that of Fig. 13.

13 Fig. 15 shows the Fig. 13 wafer fragment at a processing step
14 subsequent to that of Fig. 14.

15 Fig. 16 shows the Fig. 13 wafer fragment at a processing step
16 subsequent to that of Fig. 15.

17 Fig. 17 is a schematic, fragmentary, cross-sectional view of a
18 semiconductor wafer fragment in process according to a second
19 embodiment method of the present invention. The wafer fragment of
20 Fig. 16 is shown at a processing step subsequent to the prior art
21 processing step of Fig. 4.

22 Fig. 18 shows the Fig. 17 wafer fragment at a processing step
23 subsequent to that of Fig. 17.

1 Fig. 19 shows the Fig. 17 wafer fragment at a processing step
2 subsequent to that of Fig. 18.

3 Fig. 20 shows the Fig. 17 wafer fragment at a processing step
4 subsequent to that of Fig. 19.

5 Fig. 21 shows the Fig. 17 wafer fragment at a processing step
6 subsequent to that of Fig. 20.

7 Fig. 22 is a schematic, fragmentary, cross-sectional view of a
8 semiconductor wafer fragment in process according to a third embodiment
9 method of the present invention. The wafer fragment of Fig. 20 is
10 shown at a processing step subsequent to the prior art processing step
11 of Fig. 4.

12 Fig. 23 shows the Fig. 22 wafer fragment at a processing step
13 subsequent to that of Fig. 22.

14 Fig. 24 shows the Fig. 22 wafer fragment at a processing step
15 subsequent to that of Fig. 23.

16 Fig. 25 shows the Fig. 22 wafer fragment at a processing step
17 subsequent to that of Fig. 24.

18 Fig. 26 is a schematic, fragmentary, cross-sectional view of a
19 semiconductor wafer fragment in process according to a fourth
20 embodiment method of the present invention. The wafer fragment of
21 Fig. 26 is shown at a processing step subsequent to the prior art
22 processing step of Fig. 3.
23

1 Fig. 27 shows the Fig. 26 wafer fragment at a processing step
2 subsequent to that of Fig. 26.

3 Fig. 28 shows the Fig. 26 wafer fragment at a processing step
4 subsequent to that of Fig. 27.

5 Fig. 29 shows the Fig. 26 wafer fragment at a processing step
6 subsequent to that of Fig. 28.

7 8 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

9 This disclosure of the invention is submitted in furtherance of the
10 constitutional purposes of the U.S. Patent Laws "to promote the progress
11 of science and useful arts" (Article 1, Section 8).

12 The present invention encompasses methods which can alleviate the
13 dips 32 described above with reference to the prior art processing shown
14 in Figs. 1-12. A first embodiment of the present invention is described
15 with reference to Figs. 13-16. In describing the first embodiment, similar
16 numbering to that utilized above in describing the prior art processing
17 of Figs. 1-12 will be used, with differences indicated by suffix "a" or by
18 different numerals.

19 Fig. 13 illustrates a semiconductor wafer fragment 10a at a
20 preliminary stage of the first embodiment method. Specifically, wafer
21 fragment 10a is illustrated at a processing step subsequent to the prior
22 art step of Fig. 3. Wafer fragment 10a comprises a semiconductive
23 substrate 12, an oxide layer 14, a nitride layer 16, and a photoresist

layer 18. Openings 40 extend through oxide layer 14 and nitride layer 16 and into substrate 12. Oxide layer 14 and nitride layer 16 ultimately function as masking layers during formation of an isolation region, and so can be referred to as a first masking layer 14 and a second masking layer 16.

The formation of openings 40 can be initiated by processing identical to that described above with reference to prior art Fig. 3. Specifically, openings 20 (Fig. 3) are formed by transferring a pattern from photoresist layer 18 through first and second masking layers 14 and 16. Openings 20 (Fig. 3) are then extended into openings 40 by etching photoresist layer 18. Such etching reduces a horizontal width of photoresist layer 18 and thereby exposes portions of underlying second masking layer 16. The etch of photoresist layer 18 can comprise, for example, a dry etch utilizing a mixture of an oxygen-containing material and He. The oxygen-containing material can comprise, for example, O_2 present in a concentration greater than or equal to about 10%. Alternatively, the etch can be a dry etch utilizing 100% O_2 . The etch will generally remove photoresist faster with higher concentrations of O_2 utilized in the etch than with lower concentrations of O_2 . In embodiments in which masking layers 14 and 16 comprise oxide and nitride, respectively, the above-described etch conditions can also remove polymer from exposed portions of nitride layer 16 and oxide layer 14. Such polymer is described in the "Background" section of this disclosure

1 with reference to Fig. 3, and is described as protecting nitride
2 sidewalls 17 and oxide sidewalls 15 during a silicon etch described with
3 reference to Fig. 4. Accordingly, removal of such polymer layer can
4 increase susceptibility of layers 14 and 16 to a subsequent silicon etch.

5 Referring to Fig. 14, wafer fragment 10a is subjected to a silicon
6 etch, such as, for example, the HBr etch described above with reference
7 to Fig. 4. Such etch extends openings 40 into substrate 12 and also
8 removes exposed portions of nitride layer 16 and oxide layer 14.
9 Accordingly, the etch moves a furthest lateral periphery of the second
10 masking layer (defined by sidewalls 17) outward from the opening
11 without reducing a thickness of the second masking layer. After the
12 etching, openings 40 comprise a step 42 (corresponding to rounded
13 corners) below oxide layer 14. Step 42 defines a region where a wider
14 upper portion of an opening 40 joins to a narrower lower portion of the
15 opening 40.

16 Referring to Fig. 15, photoresist layer 18 (Fig. 14) is removed and
17 an oxide layer 44 is thermally formed within openings 40 by, for
18 example, a process analogous to that discussed above with reference to
19 the prior art wafer fragment of Fig. 5. An exemplary process for
20 thermally growing oxide is to expose wafer fragment 10a to a mixture
21 of Ar and O₂, at a temperature of about 1050°C and a pressure of
22 about 1 atmosphere, for a time of from about 10 to about 15 minutes.
23 After the formation of oxide layer 44, subsequent processing analogous

1 to that discussed above with reference to Fig. 6-12 can then be
2 conducted to form isolation regions within openings 40.

3 Fig. 16 illustrates wafer fragment 10a after such subsequent
4 processing. Specifically, Fig. 16 shows wafer fragment 10a after isolation
5 regions 46 have been formed within openings 40 (Fig. 15), and after a
6 polysilicon layer 38 is provided over the isolation regions. As shown,
7 steps 42 define an outer lateral periphery of isolation regions 46. Such
8 outer periphery is further outward than an outward periphery 33 of
9 isolation regions 30 of Fig. 12. Such has resulted in the alleviation
10 (shown as elimination) of dips 32 (Fig. 12) of the prior art isolation
11 regions.

12 A second embodiment method of the present invention is described
13 with reference to Figs. 17-21. In describing the second embodiment,
14 similar numbering to that utilized in describing the prior art of
15 Figs. 1-12 will be used, with differences indicated by the suffix "b" or by
16 different numerals.

17 Referring to Fig. 17, a wafer fragment 10b is illustrated at a
18 preliminary processing step of the second embodiment method.
19 Specifically, wafer fragment 10b is illustrated at a processing step
20 subsequent to the prior art step illustrated in Fig. 4, with photoresist
21 layer 18 (Fig. 4) having been removed. Wafer fragment 10b comprises
22 silicon substrate 12, oxide layer 14, and nitride layer 16, with layers 14
23 and 16 alternatively being referred to as first and second masking layers,

1 respectively. Openings 50 extend through nitride layer 16 and oxide
2 layer 14, and into substrate 12. Openings 50 can be formed in
3 accordance with the methods described above with reference to Fig. 4
4 for forming openings 20.

5 Referring to Fig. 18, wafer fragment 10b is exposed to a wet etch
6 which isotropically etches nitride layer 16 relative to oxide layer 14 and
7 silicon substrate 12. Such etch can comprise, for example, a dip of
8 wafer fragment 10b into phosphoric acid (H_3PO_4) at a temperature
9 of 150°C and ambient pressure. Such dip has been found to consistently
10 etch silicon nitride at a rate of about 55 Angstroms per minute. The
11 etch reduces a thickness of nitride layer 16 and at the same time moves
12 sidewalls 17 of nitride layer 16 outwardly from openings 50 to widen a
13 top portion of openings 50. The nitride etch thus results in the
14 formation of steps 52 within openings 50. Steps 52 define a location
15 where a wider upper portion of openings 50 joins a narrower lower
16 portion of openings 50. Steps 52 have an upper surface comprising
17 silicon oxide of oxide layer 14.

18 Preferably, nitride layer 16 has a thickness of at least about
19 600 Angstroms over substrate 12 after the above-discussed phosphoric
20 acid etch. If remaining nitride layer 16 is less than 600 Angstroms
21 thick, it is found to be less capable of functioning as an etch stop for
22 subsequent etching (such as the etching described with reference to prior
23 art Fig. 7). Typically, from about 50 Angstroms to about 250 Angstroms

1 of nitride is removed from nitride layer 16 during the phosphoric acid
2 etch.

3 Referring to Fig. 19, substrate 10b is exposed to a hydrofluoric
4 acid etchant to selectively remove portions of pad oxide layer 14. The
5 removal of portions of pad oxide 14 drops steps 52 to an upper surface
6 of substrate 12. In some applications, it can be equally preferable to
7 forego such pad oxide etch and proceed directly to the oxidation
8 described with reference to Fig. 20.

9 Referring to Fig. 20, wafer fragment 10b is exposed to oxidizing
10 conditions which form an oxide layer 56 within openings 50. Oxide
11 layer 56 overlies steps 52.

12 Referring to Fig. 21, wafer fragment 10b is exposed to subsequent
13 processing analogous to the prior art processing described above with
14 reference to Figs. 6-12 to form isolation regions 58 and a polysilicon
15 layer 38 overlying isolation regions 58. As shown, steps 52 define an
16 outer lateral periphery of isolation regions 58. Such outer periphery is
17 further outward than an outer periphery 33 of isolation regions 30 of
18 Fig. 12. Such has resulted in the alleviation (shown as elimination) of
19 dips 32 (Fig. 12) of the prior art isolation regions.

20 A third embodiment of the invention is described with reference
21 to Figs. 22-25. In describing the third embodiment, similar numbering
22 to that utilized above in describing the first two embodiments will be
23

used, with differences indicated by the suffix "c" or by different numerals.

Referring to Fig. 22, a wafer fragment 10c is shown at a preliminary stage of the third embodiment processing. Wafer fragment 10c is shown at a processing step subsequent to that of Fig. 4, with a photoresist layer 18 (Fig. 4) having been removed. Wafer fragment 10c comprises a semiconductor substrate 12, a pad oxide layer 14, and a silicon nitride layer 16, with layers 14 and 16 alternatively being referred to as first and second masking layers, respectively. Openings 60 extend through layers 16 and 14, and into substrate 12.

Referring to Fig. 23, nitride layer 16 is subjected to a facet etch to reduce a thickness of portions of nitride layer 16 proximate edges 17. The facet etching can comprise, for example, a plasma etch utilizing argon in combination with a fluorine-containing compound (e.g., CH_2F_2). Preferably, the mixture of argon and fluorine-containing gas comprises less than or equal to about 5% fluorine-containing gas (by volume). An exemplary pressure condition of the facet-etching is from about 2 mTorr to about 20 mTorr.

Either before or after the facet etching, wafer fragment 10c is subjected to HF etching to remove portions of oxide layer 14 from under edges 17 of nitride layer 16. The removal of the portions of

oxide layer 14 leaves exposed corners 61 of an upper surface of silicon substrate 12.

Referring to Fig. 24, wafer fragment 10c is subjected to oxidation which forms an oxide layer 62 within openings 60. The facet etching of nitride layer 16 prior to thermal oxidation results in rounding of corners 61 due to lifting of the edges of faceted nitride layer 16. The rounding of corners 61 is more pronounced than rounding of any analogous corners in the prior art processing described above with reference to Fig. 5.

Subsequent processing analogous to the prior art processing of Figs. 6-12 results in a structure shown in Fig. 25 comprising isolation regions 64 and a polysilicon layer 66 overlying isolation region 64. It is noted that the faceted edges of nitride layer 16 can lead to overhanging oxide ledges (not shown) of the isolation oxide formed during application of the subsequent processing of Figs. 6-12 to the structure of Fig. 24. If such overhanging oxide ledges are formed, they are preferably removed prior to formation polysilicon layer 66. Such overhanging oxide ledges can be removed by, for example, chemical-mechanical polishing of the isolation oxide.

Fig. 25 illustrates that rounded corners 61 have alleviated formation of dips 32 (Fig. 12) of the prior art.

A fourth embodiment of the present invention is described with reference to Figs. 26-29. In describing the fourth embodiment, similar

1 numbering to that utilized above in describing the first three
2 embodiments will be used, with differences indicated by the suffix "d" or
3 by different numerals.

4 Referring to Fig. 26, a wafer fragment 10d is shown at a
5 preliminary stage of the fourth embodiment method. Specifically, wafer
6 fragment 10d is shown at a processing step subsequent to the prior art
7 processing step of Fig. 3. Wafer fragment 10d comprises a substrate 12,
8 a pad oxide layer 14 and a nitride layer 16, with layers 14 and 16
9 alternatively being referred to as first and second masking layers,
10 respectively. Additionally, substrate 12 comprises a photoresist layer 18
11 and openings 70 extending through layers 18, 16 and 14, and into
12 substrate 12. Openings 70 can be formed by, for example, prior art
13 methods described above for forming openings 20 of Fig. 3. After
14 formation of openings 70, photoresist layer 18 is etched back by, for
15 example, a dry etch utilizing an oxygen-containing material, such as the
16 etch described above with reference to Fig. 13. Such etch exposes
17 portions of nitride layer 16, while leaving other portions covered by
18 photoresist 18.

19 Referring to Fig. 27, the exposed portions of nitride layer 16 are
20 exposed to addition etching conditions, such as, for example, a
21 phosphoric acid etch as described above with reference to Fig. 18, to
22 reduce a thickness of the exposed portions of the nitride layer.
23 Specifically, the original nitride layer had a thickness of "A" (which

1 remains the thickness of an unetched central region of the nitride layer),
2 and the etched portion of the nitride layer (the edge regions) has a
3 thickness of "B". Preferably, "B" is about one-half "A". The etching
4 does not move the furthest lateral periphery of nitride layer 16 (defined
5 by sidewall 17) outward from openings 70.

6 Referring to Fig. 28, wafer fragment 10d is exposed to oxidizing
7 conditions which grow an oxide layer 72 within openings 70. The
8 thinned regions of nitride layer 16 are relatively easily lifted by the
9 growing oxide such that "birds beaks" are formed under the thinned
10 regions of nitride layer 16. The birds beaks are extended relative to any
11 birds beaks formed during the prior art processing described above with
12 reference to Fig. 5. Photoresist layer 18 is removed prior to the
13 exposure of wafer fragment 10d to oxidizing conditions.

14 Referring to Fig. 29, wafer fragment 10d is exposed to subsequent
15 processing conditions analogous to the prior art processing described
16 above with reference to Figs. 6-12 to form isolation regions 74 and
17 polysilicon layer 38 overlying isolation regions 34. It is noted that the
18 reduced-thickness edges of nitride layer 16 can lead to overhanging oxide
19 ledges (not shown) of the isolation oxide formed during application of
20 the subsequent processing of Figs. 6-12 to the structure of Fig. 27. If
21 such overhanging oxide ledges are formed, they are preferably removed
22 prior to formation polysilicon layer 38. Such overhanging oxide ledges
23

1 can be removed by, for example, chemical-mechanical polishing of the
2 isolation oxide.

3 The processing of Figs. 26-29 alleviates the prior art dips 32
4 described above in the "Background" section (shown as elimination of
5 dips 32).

6 In compliance with the statute, the invention has been described
7 in language more or less specific as to structural and methodical
8 features. It is to be understood, however, that the invention is not
9 limited to the specific features shown and described, since the means
10 herein disclosed comprise preferred forms of putting the invention into
11 effect. The invention is, therefore, claimed in any of its forms or
12 modifications within the proper scope of the appended claims
13 appropriately interpreted in accordance with the doctrine of equivalents.
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